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CBCS SCHEME

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BEC/BTE/BVL654A

Sixth Semester B.E./B.Tech. Degree Examination, June/July 2026
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M: Marks, L: Bloom's level, C: Course outcomes.

			M	L	C
		Module – 1			
Q.1	**a.**	Briefly explain about the importance of HDL and trends in HDL.	**10**	**L2**	**CO1**
	b.	Explain the typical VLSI design flow with a neat flow diagram.	**10**	**L2**	**CO1**
		OR			
Q.2	**a.**	Define module and an instance. Briefly explain any two description styles of verilog HDL.	**10**	**L2**	**CO1**
	b.	With a neat block diagram explain top-down design and bottom up design methodologies.	**10**	**L2**	**CO1**
		Module – 2			
Q.3	**a.**	Define the following data types with example. i) Nets ii) Registers iii) Vectors iv) Array v) Parameter	**10**	**L2**	**CO1**
	b.	Explain the following lexical conventions with example. i) Comments ii) Operator iii) Sized numbers iv) X or Z values v) Strings	**10**	**L2**	**CO1**
		OR			
Q.4	**a.**	Explain how ports are connected to external signals.	**10**	**L2**	**CO1**
	b.	With a neat block diagram explain components of verilog module.	**10**	**L2**	**CO1**

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		Module – 3			
Q.5	**a.**	With the help of logic diagram, write verilog code for 4:1 MUX using gate level modeling and also write the stimulus.	**10**	**L3**	**CO3**
	b.	What are rise, fall and turn off delays? Write the statements for delay time for all transitions, rise and fall delay specification and rise, fall and turn off delay with examples.	**10**	**L2**	**CO3**
		OR			
Q.6	**a.**	Write the verilog code for the design block and the stimulus block of a 4 bit ripple carry full adder.	**10**	**L3**	**CO3**
	b.	Explain the following operator with an example: i) Logical ii) Replication iii) Shift iv) Conditional v) Bitwise	**10**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	Write a verilog behavioral description of 8:1 MUX using core statement.	**10**	**L3**	**CO4**
	b.	Explain the blocking assignment statements and non blocking assignment statements with relevant examples.	**10**	**L2**	**CO4**
		OR			
Q.8	**a.**	Write verilog behavioral description of a 4 bit binary counter.	**10**	**L3**	**CO4**
	b.	Explain sequential and parallel blocks with example.	**10**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Write any 5 differences between verilog tasks and functions.	**10**	**L2**	**CO4**
	b.	Write the verilog structural description for a 2:4 decoder with tristate output. Write the truth table, logic diagram and simulation waveforms.	**10**	**L3**	**CO5**
		OR			
Q.10	**a.**	Write the syntax along with an example for the following: i) Task Declaration and Invocation ii) Function Declaration and Invocation	**10**	**L2**	**CO4**
	b.	Write the structural description of a 2×1 multiplexes with active low enable.	**10**	**L3**	**CO4**

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